Abstract

Techniques are disclosed for implementing software breakpoints in a multiprocessor system having a number of processors each coupled to a main memory. In an illustrative embodiment, each of the processors has an instruction cache associated therewith. An instruction for which a breakpoint is to be inserted is retrieved from a corresponding instruction address in the main memory, and a breakpoint code, e.g., a debug opcode, is inserted at the instruction address in main memory. After the breakpoint code is executed by a given one of the processors, the retrieved instruction is stored in the corresponding instruction cache for that processor, and a use-once indicator, associated with the instruction as stored in the corresponding instruction cache for that processor, is set. The use-once indicator, when set for the instruction as stored in the instruction cache, is operative via cache control logic to clear a validity indicator associated with the instruction after a single fetch of the instruction from the instruction cache, such that subsequent attempts by the given processor to access the instruction as stored in the instruction cache will cause the processor to retrieve the breakpoint code at the instruction address in main memory. As a result, the desired breakpoint code will remain present in the main memory, such that all of the processors of the system can reliably fetch and execute that code even if one or more of these processors are resuming execution from the breakpoint.